CLAIMS

What is claimed is:

1. A load detector circuit system, comprising:

a digital-to-analog converter (DAC) comprising a differential architecture comprising a first output and a second output working in opposite phase;

an output circuit coupled to said first output, said output circuit configured to drive an external load;

a dumping circuit coupled to said second output configured such that said dumping circuit is balanced with said output circuit when said external load is coupled to said output circuit; and

a determining circuit for examining a first voltage on said first output and a second voltage on said second output to determine if said dumping circuit is balanced with said output circuit.

2. The load detector circuit of Claim 1, wherein said determining circuit comprises:

an adding circuit to calculate a summed voltage of said first voltage and said second voltage; and

a comparator for comparing said summed voltage to a reference voltage.

3. The load detector circuit of Claim 2, wherein said reference voltage comprises a direct current (DC) voltage.

4. The load detector circuit of Claim 2, wherein said reference voltage comprises a fixed DC level.

5. The load detector circuit of Claim 2, wherein said summed voltage comprises a constant DC value and essentially equals said reference voltage when said external load is coupled to said output circuit.

6. The load detector circuit of Claim 2, wherein said summed voltage does not equal said reference voltage and comprises a DC component and an AC component when said external load is not coupled to said output circuit.

7. The load detector circuit of Claim 2, wherein said determining circuit uses the presence of a DC component in said summed voltage to determine that said external load is present.

8. The load detector circuit of Claim 2, wherein said determining circuit uses the presence of an AC component in said summed voltage to determine that said external load is not present.

9. The load detector circuit of Claim 1, wherein said output circuit comprises:

a resistor coupled to said first output and to ground;

a filter coupled to said first output; and

a connector coupled to said filter, wherein said connector is configured to receive said external load.

10. The load detector circuit of Claim 9, wherein said resistor in parallel with a load resistance associated with said external load are balanced with a second resistance associated with said dumping circuit.

11. The load detector circuit of Claim 1, wherein said determining circuit examines said first voltage and said second voltage independently of video content on said video DAC.

12. The load detector circuit of Claim 1, further comprising:

a controller for disabling said video DAC when said external load is not coupled to said output circuit.

13. The load detector circuit of Claim 1, wherein said determining circuit comprises:

a comparator for comparing said first voltage and said second voltage, such that said first voltage is equal to said

second voltage when said output circuit and said dumping circuit is balanced.

14. The load detector circuit of Claim 13, wherein said comparator is driven to half scale.

15. A method for detecting a load, comprising:

a) calculating a summed voltage of a first voltage from a first output and a second voltage from a second output of a digital-to-analog converter (DAC) that is enabled, wherein said first output and said second output work in opposite phase, and wherein said first output is coupled to an output circuit configured to receive an external load; and

b) determining if a dumping circuit coupled to said second output is balanced with said output circuit to determine if said external load is present, wherein said dumping circuit is balanced with said output circuit when said external load is coupled to said output circuit.

16. The method of Claim 15, wherein said c) comprises:

comparing said summed voltage to a direct current (DC) reference voltage.

17. The method of Claim 16, further comprising:

determining said dumping circuit is balanced with said output circuit when said summed voltage substantially

comprises a DC component and is equal to said DC reference voltage.

18. The method of Claim 16, further comprising:

determining said dumping circuit is not balanced with said output circuit when said summed voltage is not equal to said DC reference voltage, wherein said summed voltage comprises a DC component and an alternating current (AC) component.

19. The method of Claim 18, wherein said summed voltage is greater than said DC reference voltage when said dumping circuit is not balanced with said output circuit.

20. The method of Claim 16, further comprising:

d) determining if said first output is overloaded by said external load and another external load, when said first voltage is less than said second voltage.

21. The method of Claim 15, wherein said c) comprises:

comparing a first voltage at said first output and a second voltage at said second output.

22. The method of Claim 15, further comprising:

d) disabling said video DAC when said dumping circuit is not balanced with said output circuit.

23. The method of Claim 21, further comprising:

e) enabling said video DAC that is disabled to determine if said external load is coupled to said output circuit.

24. A load detector circuit, comprising:

a digital-to-analog converter (DAC) comprising a differential architecture comprising a first output and a second output working in opposite phase;

a buffer circuit coupled to said first output and said second output of said video DAC, said buffer circuit comprising a buffer output coupled to a resistor and a connector in series, wherein said connector is configured to receive an external load;

a summing circuit for calculating a summed voltage of a first voltage at said connector and a second voltage at said second output; and

a comparator circuit for determining when said summed voltage indicates said external load is present.

25. The load detector circuit of Claim 24, wherein said buffer circuit further comprises:

an operational amplifier comprising a non-inverting input, an inverting input, and said buffer output, wherein said non-inverting input is coupled to a first resistor and said first output in series, and wherein said inverting input

is coupled to a third resistor and said second output in series;

a second resistor coupled to said non-inverting input and to ground; and

a feedback resistor coupled to said inverting input and to said buffer output.

26. The load detector circuit of Claim 24, wherein said comparator circuit determines said external load is present when said summed voltage equals one half of a full scale voltage, wherein said full scale voltage comprises the sum of said second voltage and an output voltage at said first output.

27. The load detector circuit of Claim 24, wherein said comparator circuit determines said external load is not detected when said summed voltage equals a output voltage at said first output.

28. The load detector circuit of Claim 24, wherein said DAC comprises a video DAC.